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Printed Organic Photovoltaic Device with Buffer Layers

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Abstract: Fully printed organic photovoltaic (OPV) devices were fabricated using slot die coating, electro-spraying, and screen printing technologies. A fundamental study was performed to fabricate the organic photovoltaic device with the functional layers. In order to minimize the decrease of the device performance caused by printing, electron and hole extraction buffers were inserted. The insertion of the ethoxylated polyethylenimine electron extraction buffer layer between the cesium-doped TiO_2 layer and active layer helped electron extraction by reducing the inter-layer resistance. The insertion of a photo-curable hole extraction buffer layer between the active layer and metal electrode helped to reduce the leakage current. The series resistance decreased and the shunt resistance increased with the insertion of this hole extraction layer. The electron and hole extraction buffer layers improved the device performance of the printed OPV device.

Keywords: printing, slot die, organic photovoltaic, buffer layer.

Introduction

Organic photovoltaic (OPV) devices have several advantages over traditional silicon-based or other inorganic solar cells including the possibility of a custom tailored structure as well as their light weight, inexpensive, and reproducible processability properties. The best advantage of OPV devices over their inorganic counterparts is that they can be fabricated in a low cost flexible form by printing technology. The good solubility characteristics of polymers are suitable for the flexible device manufacturing process employing printing technology. Recently, many researchers have focused on the utilization of mass production capable roll-to-roll processing to reduce the production cost.[1,2] Roll-to-roll processing technology, with its high production throughput, is recognized as a method for low-cost mass production of large-area flexible organic electronics.[3-7] Organic solar cells are usually fabricated as a module and their efficiency is significantly reduced compared to devices prepared by a laboratory scale unit cell.

It is possible to utilize small organic semiconductor materials to fabricate a high performance device containing multi-functional layers, such as an injection layer and a transporting layer, by thermal evaporation. The device efficiency resulting from thermal evaporation is usually high since sublimation (the process used for thermal evaporation) is a very good purification process for organic materials. The fabrication process utilizing a polymer has advantages in that not only is the solution process possible at low temperatures but mass production is also possible using a roll-to-roll process. However, the device efficiency is low due to the impossibility of thermal evaporation and the difficulty of polymer purification. The device also exhibits a lower efficiency because the organic functional layers cannot be overlayed due to solvent similarity in the solution process. In particular, when the solution process is used in the fabrication of OPV devices, the fill factor and V_{oc} generally decrease.

In this study, a fundamental study was performed to fabricate an OPV device with functional layers, which can be used to avoid the weaknesses of polymer solution processes. The multi-layer overlayed structures were fabricated using an electro-spraying process. The functional layer resulted in an improved open circuit voltage, fill factor, and resistances (decreasing series and increasing shunt).

Experimental

A patterned ITO cell with an insulator was prepared by photolithography and cleaned using acetone, isopropyl alcohol, and deionized water, sequentially. The cleaned ITO was then treated with UV-ozone to result in better coating characteristics. Cesium-doped TiO_2 was prepared by mixing 2 wt% TiO_2/ethanol with 0.2 wt% Cs/2-ethoxyethanol, as reported elsewhere.[8] The prepared Cs:TiO_2 was slot-coated using the following parameters: a flow rate of 0.2 mL/s, a shim plate thickness of 40 μm, a coating speed of 1 mm/s, and a head to substrate distance of 100 μm. The resulting thickness was

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about 0.6 μm. The coated electron extraction layer was annealed at 80 °C for 1 min and dried in a vacuum oven at 110 °C for 10 min. An electron extraction buffer layer was formed using 1 wt% ethoxylated polyethylenimine (PEIE, Sigma-Aldrich, M_w=75,000) in a mixed solvent of methoxyethanol and tetrachloroethane. The thickness of PEIE was about 20 nm. PEIE was annealed at 50 °C for 5 min. 6 wt% of regioregular poly [3-hexylthiophene-2,5-diyl] (P3HT) (Solaris) and PCBM (Nano-C) blended at a 5:3 weight ratio was dissolved in chlorobenzene and slot die-coated onto ITO coated with an electron extraction layer. The coating conditions included a flow rate of 0.1 mL/s, a coating speed of 10 mm/s, and a head to substrate distance of 75 μm. The coated active layer was annealed at 80 °C for 1 min and dried in a vacuum oven at 150 °C for 10 min. The thickness of the active layer was about 200 nm. PEDOT:PSS (Agfa EL-P5010) was mixed with isopropyl alcohol at a 1:1 weight ratio so that the viscosity was less than 2,000 cP. PEDOT:PSS was coated using a slot die with a flow rate of 0.2 mL/s. The other processing parameters included a shim plate thickness of 40 μm, a coating speed of 6 mm/s, and a head to substrate distance of 100 μm. The coated PEDOT:PSS layer was annealed at 80 °C for 1 min and the coating process was repeated up to 3 times. Once all PEDOT:PSS layers were coated, the sample was vacuum dried at 110 °C for 10 min. 0.1 wt% photo-curable precursor was prepared in chlorobenzene mixed with tetrachloroethane.[9] The electro-spraying conditions included a spraying distance of 10 cm, an applied voltage of 14-15 kV, and spraying for 1 s at a capacity of 30 μL/s. The thickness of this buffer layer was about 5 nm. The photo-curable precursor was cured using a UV lamp for 3 min. The silver electrode (TOYO UV cure) was formed by screen printing and vacuum dried at 110 °C for 10 min. The thickness of the silver layer was about 20 μm.

Results and Discussion

In this study, inverted OPVs were prepared by a printing method. In order to simulate a roll-to-roll processing environment, all fabricated device layers were formed via slot die coating or screen printing. The hole transporting layer in a printed OPV is usually formed with PEDOT:PSS (Agfa E5010) which possesses a fairly high viscosity, typically above 12,000 cP. Due to the existence of nano-sized particles, the gear pump used for printing limited the maximum viscosity in our slot die coater to a few thousand cP. Therefore, PEDOT:PSS was diluted with isopropyl alcohol to reduce the viscosity. The optimum thickness of the PEDOT:PSS layer in our study was 2-4 μm. As a result, multilayer printing was carried out, as shown in Figure 1. Bar coating using transparent tape produced 1.7-3.3 μm thick PEDOT:PSS films depending on the number of layer(s). From the thickness measurement and corresponding OPV performance, the optimal layer was determined to be a triple-coated layer (1 min annealing at 80 °C for each layer). In the slot die coating of the PEDOT:PSS layer, the process conditions were a flow rate of 0.2 mL/s, a shim plate thickness of 40 μm, a coating speed of 1 mm/s, and a head to substrate distance of 100 μm. The bar-coated PEDOT:PSS OPV cell and slot die-coated PEDOT:PSS OPV cell showed similar performances under AM 1.5 conditions. The open circuit voltage, short circuit current, fill factor, and efficiency of the bar-coated OPV cell were 0.594 V, 7.33 mA/cm^2, 0.489, and 2.13%, respectively. The corresponding values for the slot die-coated OPV cell were 0.564 V, 7.76 mA/cm^2, 0.486, and 2.13%, respectively. The series resistances of the bar-coated and slot die-coated devices were 731 and 650 Ω, respectively. The shunt resistances of the bar-coated and slot die-coated devices were 10,800 and 8,025 Ω, respectively. The most noticeable difference between the bar-coated cell and slot die-coated cell was the shunt resistance. The series resistance originates from the resistance characteristics against charge following each layer, the resistance of the electrodes, and the contact resistance between layers, while the shunt resistance originates from defects in the manufacturing process and leakage current. According to experimental data, when the thickness of PEDOT:PSS was thin, this buffer layer could be penetrable by the solvent included in Ag paste. The bar coated buffer layer which was much thicker than the slot die coated (bar coated PEDOT:PSS was about 3.5 μm), while slot die coated about 2 μm as shown in Figure 1. Due to the penetration of silver metal clusters into the PEDOT:PSS, the leakage current flows in the case of thinner buffer layer so that the shunt current was lower for the slot die coated device. From these results, it is obvious that a modification process which can block the leakage current of the slot die-coated PEDOT:PSS layer is required.

In this study, doped metal oxide nanoparticle and photo-curable buffer layers were used for enhancement of the performance of the printed OPV cell. Figure 2 shows (a) the device structures used in this study and (b) the corresponding energy diagrams. The device is composed of a hole and electron extraction interlayers that can help block the leakage current and diode characteristics. The insertion of a PEIE layer between

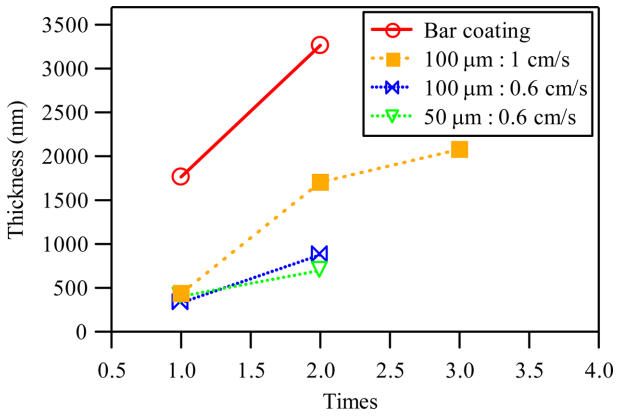

Figure 1. Thicknesses of the printed PEDOT:PSS layers.

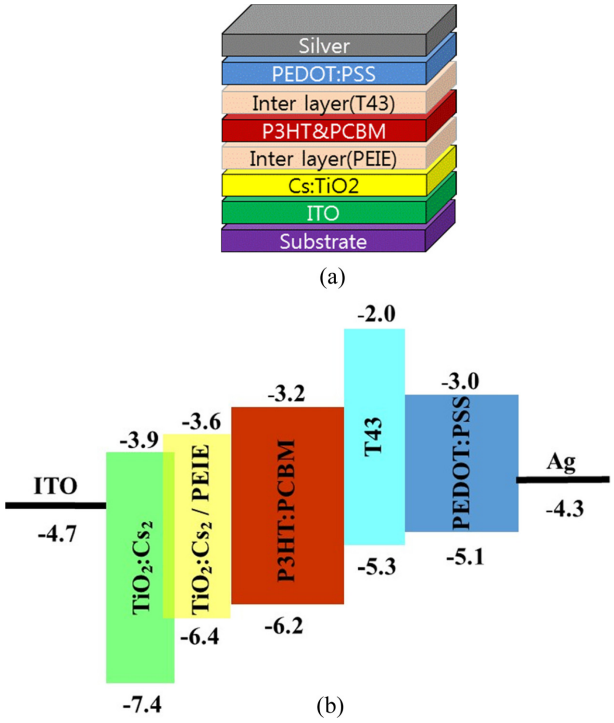

Figure 2. (a) Device structures evaluated in this study and (b) corresponding energy diagrams.

the cesium-doped TiO_2 layer and the active layer is supposed to help electron extraction by reducing the interlayer resistance. The insertion of a photo-curable layer between the PEDOT:PSS layer and active layer is supposed to help hole extraction by reducing the interlayer resistance. PEIE is frequently used as a modified layer to obtain a low work function electrode.[10] Many studies have been performed to address the difficulty of energy level matching between the work function of the cathode and the LUMO of the semiconducting acceptor. The doping of Cs in the TiO_2 layer has also been frequently studied since cesium doping can stabilize the nanostructure morphology of TiO_2 and enhance efficient electron extraction and blocking of holes. As a result, cesium doping increases the fill factor and open circuit voltage. The photo-curable hole buffer layer was coated by electro-spraying and photo-cured for the formation of an insoluble interlayer. This photo-curable interlayer acted as a leakage current reducing buffer layer. Because of the reduction of the fill factor and open circuit voltage for the printed OPV cell, some buffer layers are required. The fabrication of an organic buffer layer on top of the active layer is difficult in printing processes due to solvent similarity of the solution processes. Therefore, the hole extraction buffer layer was coated by an electro-spraying method, which has less dissolution problems for the pre-existing layer since the solvent included in the printing solution would evaporate in the traveling distance from the spraying tip to the substrate. This electro-spraying process also demonstrates uniform and ultrathin layer coating fabrication capability.

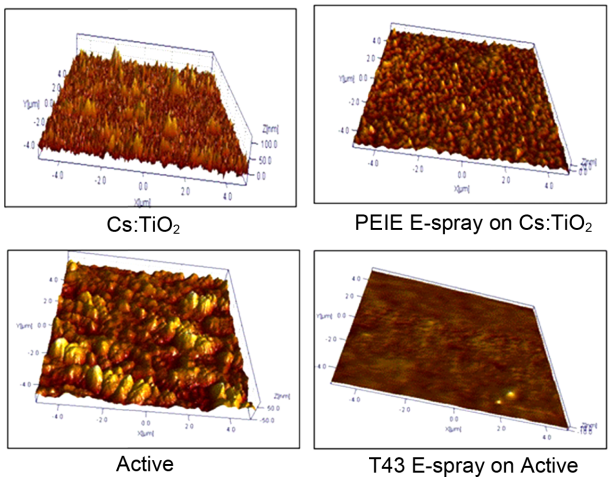

Figure 3. The surface morphologies of the printed layers.

Figure 3 shows the surface morphology of each layer. As shown in the figure, the root mean square (RMS) roughnesses of the TiO_2 and TiO_2:Cs films were 24 and 11.7 nm, respectively. As reported elsewhere,[8] cesium doping stabilizes the nanostructure morphology of TiO_2 so that the mean roughness of cesium-doped TiO_2 was smoother compared to the bare TiO_2 film. The roughness of the TiO_2:Cs film changed to 5.35 nm as the PEIE layer was over-coated on the top of TiO_2:Cs. Even though the thickness of the PEIE layer is normally very thin, this buffer layer smooths the roughness of the TiO_2:Cs film. After coating the active layer, the mean roughness was quite high due to phase separation of P3HT:PCBM by thermal annealing. The RMS roughness of the active layer became 1.27 nm. The photo-curable buffer layer was coated on top of the active layer by electro-spraying and this buffer layer smoothed the roughness of the active layer to a very small degree.

Figure 4 shows the *J-V* characteristics of the printed OPV cells. The data is summarized in Table I. The reference device was slot-coated with a structure of ITO/TiO_2/P3HT:PCBM/Agfa

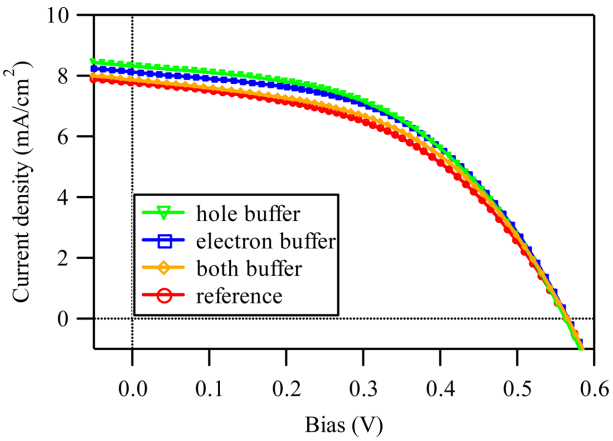

Figure 4. *J-V* characteristics of the printed OPV cells.

Table I. Device Performances with Different Buffer Layers

	V_{oc} (V)	J_{sc} (mA/cm^2)	FF	Eff. (%)	R_s (Ω)	R_{sh} (Ω)
Reference	0.564 ± 0.007	7.761 ± 0.18	0.486 ± 0.0067	2.13 ± 0.09	650 ± 15	8025 ± 805
Electron Buffer	0.566 ± 0.007	8.117 ± 0.15	0.488 ± 0.0096	2.24 ± 0.08	590 ± 15	10300 ± 1070
Hole Buffer	0.562 ± 0.006	8.314 ± 0.14	0.494 ± 0.0095	2.31 ± 0.09	585 ± 15	9950 ± 910
Both Buffer	0.565 ± 0.004	7.858 ± 0.09	0.480 ± 0.007	2.13 ± 0.08	620 ± 15	8370 ± 495

5010/Ag. The open circuit voltage, short circuit current density, fill factor, and efficiency for the bar-coated OPV reference cell were 0.564 V, 7.761 mA/cm^2, 0.486, and 2.13%, respectively. The electron extraction buffer layer (PEIE) and hole extraction buffer layer (T43) resulted in an enhanced power conversion efficiency. The device with PEIE (structure: ITO/TiO_2:Cs/PEIE/P3HT:PCBM/Agfa 5010/Ag) in the bar-coated OPV reference cell demonstrated an open circuit voltage, short circuit current density, fill factor, and efficiency of 0.566 V, 8.117 mA/cm^2, 0.488, and 2.24%, respectively. As expected, the insertion of the PEIE layer between the cesium-doped TiO_2 layer and active layer helps electron extraction by reducing the interlayer resistance (smaller energy level differences). As a result, the short circuit current density increased from 7.761 (reference device) to 8.117 mA/cm^2 with a PEIE buffer layer. The device with the photo-curable layer (structure: ITO/TiO_2:Cs/P3HT:PCBM/T43/Agfa 5010/Ag) showed an open circuit voltage, short circuit current density, fill factor, and efficiency of 0.562 V, 8.314 mA/cm^2, 0.494, and 2.31%, respectively. The series resistance decreased and the shunt resistance increased with insertion of this layer. The fill factor was the highest among the three devices (reference, with PEIE, and with T43), as summarized in Table I, which demonstrates that the photo-curable interlayer acted as a leakage current reducing buffer layer. The device with both electron and hole extraction layers (structure : ITO/TiO_2:Cs/PEIE/P3HT:PCBM/T43/Agfa 5010/Ag) showed the open circuit voltage, short circuit current density, the fill factor and the efficiency for bar coated OPV reference cell were 0.565 V, 7.858 mA/cm^2, 0.480 and 2.13%, respectively. When both buffer layers were used at the same device, the power conversion efficiency was rather decreased. PEIE which acted as an electron buffer is an insulating material. When PEIE is coated as an ETL, it would form an ohmic contact and plays role of lowering HOMO level of oxide layer.[10] This lowering causes a leakage current to be flowed. As written in Table I, the series resistance was reduced; however, the shunt resistance was also reduced, so that the power conversion efficiency was decreased than that obtained from each buffer layer.

Conclusions

For OPV applications, the most promising advantages are cheap, flexible, and large area devices. These properties can be obtained by the utilization of mass production capable roll-to-roll solution processing. However, the device efficiency is generally lower for printed OPV devices due to less adhesion and packing between the printed layer compared to that obtained from spin coating. Printed OPV devices also exhibit lower efficiencies because the functional layers cannot be overlayed due to solvent similarity in the solution process. In this study, fully printed organic photovoltaic devices were fabricated using slot die coating, electro-spraying, and screen printing technologies. Fundamental processing conditions were studied in order to fabricate an organic photovoltaic device with the functional layers. In order to minimize the device performance decrease caused by printing, electron and hole extraction buffer layers were inserted. The insertion of an electron extraction layer PEIE between the cesium-doped TiO_2 layer and active layer helped electron extraction by reducing the interlayer resistance. As a result, the short circuit current density increased from 7.761 (reference device) to 8.117 mA/cm^2 with the PEIE buffer layer. The insertion of a hole extraction photo-curable buffer layer between the active layer and metal electrode helped to reduce the leakage current. The series resistance decreased and the shunt resistance increased with insertion of this layer. The series resistance decreased from 650 (reference device) to 585 Ω with the photo-curable buffer layer and the shunt resistance increased from 8,025 (reference device) to 9,950 Ω with the photo-curable buffer layer. Combining effect of both electron and hole extraction buffer layers in the same device has to be carefully engineered to enhance the power conversion efficiency of printed OPV device.

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